**EXPERIMENT No-12**

AIM:- To write a code in VHDL for implementing the Arithmetic Logic Unit(ALU) and to verify the functionality.

PROGRAM:-library ieee;  
use ieee.std\_logic\_1164.all;  
use ieee.std\_logic\_arith.all;  
use ieee.std\_logic\_unsigned.all;  
entity alu is  
port(a,b,e: in std\_logic;

c,d: in integer;

s: in std\_logic\_vector(2 downto 0);

q: out std\_logic;

x:out integer);  
end alu;  
architecture alu1 of alu is  
begin  
process(e,a,b,c,d,s)  
begin  
if(e='0')then case s is  
when"000"=>q<= a or b;  
when"001"=>q<= a and b;  
when"010"=>q<= not a;  
when"011"=>q<= a xor b;  
when"100"=>q<= a nand b;  
when"101"=>q<= a nor b;  
when"110"=>q<= not(a xor b);

when"111"=>q<= not b;  
when others=> null;  
end case;  
elsif(e='1')then case s is  
when"000"=>x<= c+d;  
when"001"=>x<= c-d;  
when"010"=>x<= c\*d;  
when"011"=>x<= abs(c);  
when"100"=>x<= (c\*d)+1;  
when"101"=>x<= (c\*d)-1;  
when"110"=>x<= c+d+1;  
when"111"=>x<= c-d-1;  
when others=> null;  
end case;  
end if;  
end process;  
end alu1;

WAVEFORMS: